



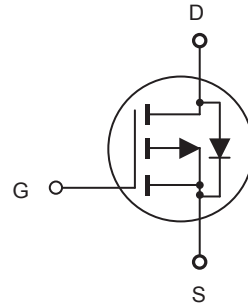
CED20P10/CEU20P10

P-Channel Enhancement Mode Field Effect Transistor

PRELIMINARY

FEATURES

- -100V, -16A, $R_{DS(ON)} = 130m\Omega$ @ $V_{GS} = -10V$.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability.
- Lead-free plating ; RoHS compliant.
- TO-251 & TO-252 package.



ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ C$ unless otherwise noted

| Parameter | Symbol | Limit | Units |
|---|----------------|------------|---------------|
| Drain-Source Voltage | V_{DS} | -100 | V |
| Gate-Source Voltage | V_{GS} | ± 20 | V |
| Drain Current-Continuous | I_D | -16 | A |
| Drain Current-Pulsed ^a | I_{DM} | -64 | A |
| Maximum Power Dissipation @ $T_C = 25^\circ C$ - Derate above $25^\circ C$ | P_D | 75 | W |
| | | 0.5 | W/ $^\circ C$ |
| Single Pulsed Avalanche Energy ^e | E_{AS} | 128 | mJ |
| Single Pulsed Avalanche Current ^e | I_{AS} | 16 | A |
| Operating and Store Temperature Range | T_J, T_{stg} | -55 to 175 | $^\circ C$ |

Thermal Characteristics

| Parameter | Symbol | Limit | Units |
|---|-----------------|-------|--------------|
| Thermal Resistance, Junction-to-Case | $R_{\theta JC}$ | 2 | $^\circ C/W$ |
| Thermal Resistance, Junction-to-Ambient | $R_{\theta JA}$ | 50 | $^\circ C/W$ |

This is preliminary information on a new product in development now .
Details are subject to change without notice

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Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|--|--------------|---|------|------|------|------------|
| Off Characteristics | | | | | | |
| Drain-Source Breakdown Voltage | BV_{DSS} | $V_{GS} = 0V, I_D = -250\mu A$ | -100 | | | V |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS} = -100V, V_{GS} = 0V$ | | | -1 | μA |
| Gate Body Leakage Current, Forward | I_{GSSF} | $V_{GS} = 16V, V_{DS} = 0V$ | | | 100 | nA |
| Gate Body Leakage Current, Reverse | I_{GSSR} | $V_{GS} = -16V, V_{DS} = 0V$ | | | -100 | nA |
| On Characteristics ^c | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{GS} = V_{DS}, I_D = -250\mu A$ | -2 | | -4 | V |
| Static Drain-Source On-Resistance | $R_{DS(on)}$ | $V_{GS} = -10V, I_D = -8A$ | | 110 | 130 | m Ω |
| Dynamic Characteristics ^d | | | | | | |
| Input Capacitance | C_{iss} | $V_{DS} = -25V, V_{GS} = 0V,$ $f = 1.0 \text{ MHz}$ | | 1260 | | pF |
| Output Capacitance | C_{oss} | | | 210 | | pF |
| Reverse Transfer Capacitance | C_{rss} | | | 40 | | pF |
| Switching Characteristics ^d | | | | | | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD} = -50V, I_D = -16A,$ $V_{GS} = -10V, R_{GEN} = 25\Omega$ | | 22 | 44 | ns |
| Turn-On Rise Time | t_r | | | 16 | 32 | ns |
| Turn-Off Delay Time | $t_{d(off)}$ | | | 85 | 170 | ns |
| Turn-Off Fall Time | t_f | | | 29 | 58 | ns |
| Total Gate Charge | Q_g | $V_{DS} = -80V, I_D = -16A,$ $V_{GS} = -10V$ | | 30 | 39 | nC |
| Gate-Source Charge | Q_{gs} | | | 6 | | nC |
| Gate-Drain Charge | Q_{gd} | | | 12 | | nC |
| Drain-Source Diode Characteristics and Maximum Ratings | | | | | | |
| Drain-Source Diode Forward Current ^b | I_S | | | | -16 | A |
| Drain-Source Diode Forward Voltage ^c | V_{SD} | $V_{GS} = 0V, I_S = -16A$ | | | -1.2 | V |
| Notes : □ a.Repetitive Rating : Pulse width limited by maximum junction temperature.□ b.Surface Mounted on FR4 Board, $t \leq 10 \text{ sec.}$ □ c.Pulse Test : Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.□ d.Guaranteed by design, not subject to production testing.□ e.L = 1mH, $I_{AS} = 16A$, $V_{DD} = 25V$, $R_G = 25\Omega$, Starting $T_J = 25 \text{ C}$ □ | | | | | | |



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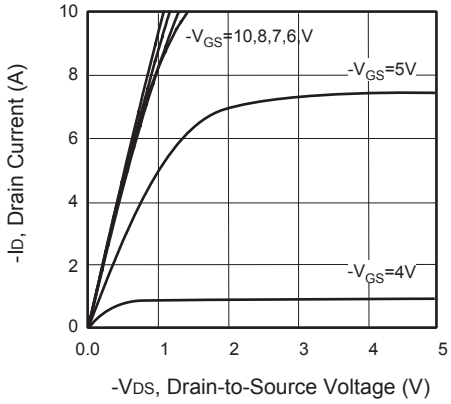


Figure 1. Output Characteristics

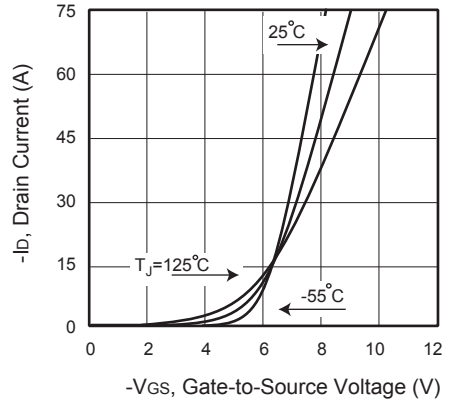


Figure 2. Transfer Characteristics

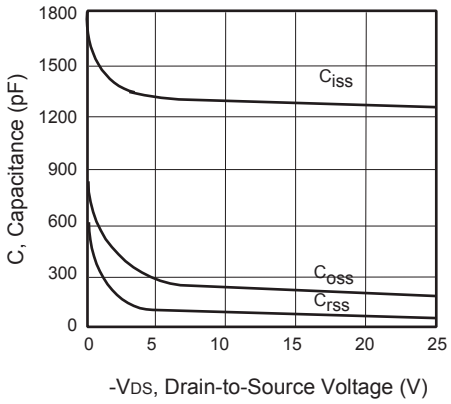


Figure 3. Capacitance

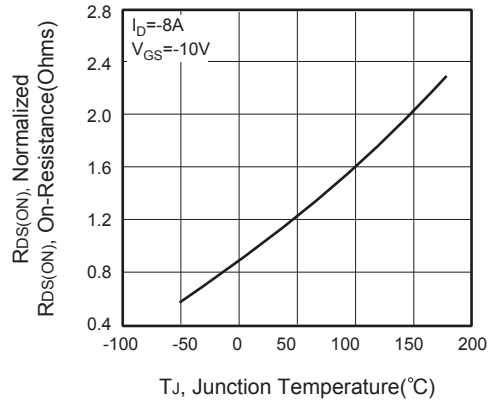


Figure 4. On-Resistance Variation with Temperature



Figure 5. Gate Threshold Variation with Temperature

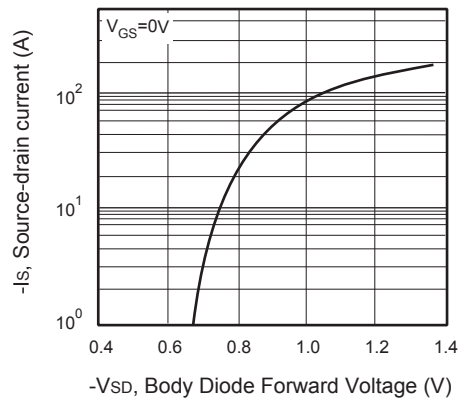


Figure 6. Body Diode Forward Voltage Variation with Source Current



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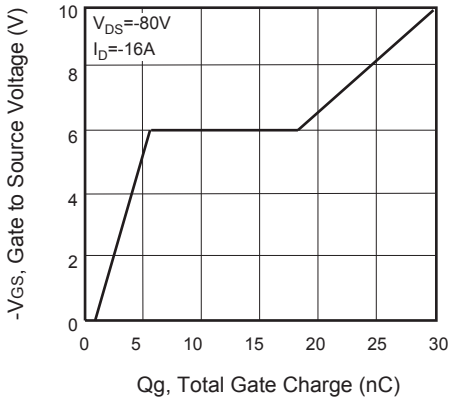


Figure 7. Gate Charge

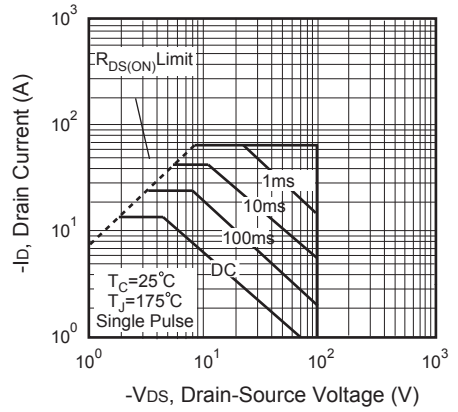


Figure 8. Maximum Safe Operating Area



Figure 9. Switching Test Circuit



Figure 10. Switching Waveforms

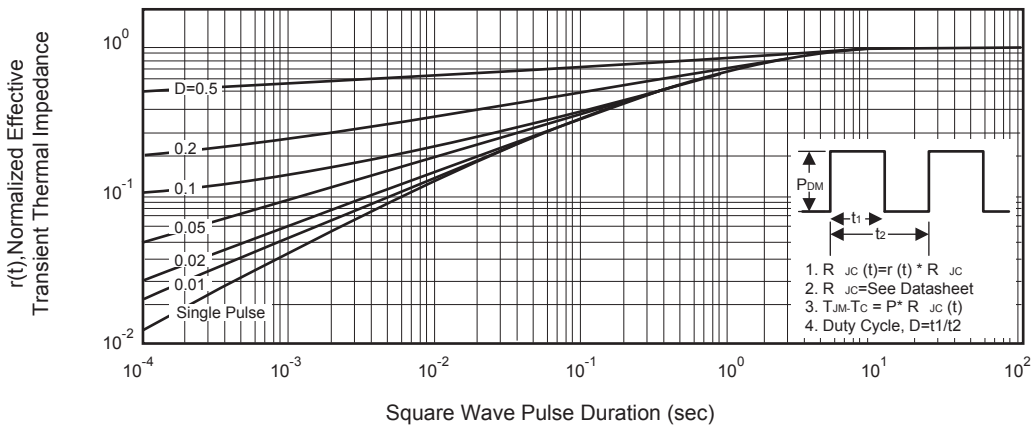


Figure 11. Normalized Thermal Transient Impedance Curve